

In the Specification:

Please replace the paragraph beginning at page 2, line 5 with the following rewritten paragraph:

In a cache-coherent system, multiple processors see a consistent view of memory. Several memory-consistency models may be implemented. The most straightforward model is called sequential consistency. Sequential consistency requires that the result of any execution be the same as if the accesses executed by each processor were kept in order and the accesses among different processors were interleaved. The simplest way to implement sequential consistency is to require a processor to delay the completion of any memory access. However, sequential consistency is generally inefficient. Figs. 1 a-c outline the process of adding a new element 30 to a data structure 5 in a sequential consistency model. Fig. 1a is an illustration of a sequential consistency memory model for a data structure prior to adding or initializing a new element 30 to the data structure 5. The data structure 5 includes a first element 10 and a second element 20. Both the first and second elements 10 and 20, respectively, have three fields 12, 14 and 16, and 22, 24 and 26. In order to add a new element 30 to the data structure 5 such that the CPUs in the multiprocessor environment could concurrently search the data structure, the new element 30 must first be initialized. This ensures that CPUs searching the linked data structure do not see fields in the new element filled with corrupted data. Following initialization of the new element's 30 fields 32, 34 and 36, the new element may be added to the data structure 5. Fig. 1b is an illustration of the new element 30 following initialization of each of its fields 32, 34 and 36, and prior to adding the new element 30 to the data structure 5. Finally, Fig. 1c illustrates the addition of the third element to the data structure following the initialization of the fields 32, 34 and 36. Accordingly, in a sequential consistency memory model execution of each step in the process must occur in a pre-specified order.